SHIFTED COMPLETELY CONNECTED NETWORK (SCCN): ARCHITECTURE OF HIERARCHICAL INTERCONNECTION NETWORK TO IMPROVE THE PERFORMANCE OF MASSIVELY PARALLEL COMPUTER SYSTEMS

BY

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ABSTRACT

At the current time, finding an alternative computing device with extreme computation power became the main concern of the research community. Therefore, building a computer device able to execute extremely difficult calculations in a short time is required. Presently, massively parallel computer (MPC) systems considered the highest computing devices, and the existence of these systems is important to execute many operations in many sectors such as engineering and science. These systems built based on an internal network called interconnection network which has a particular design represented by the network topology. The performance of these networks affected widely by the network topology. Besides, the cost of these networks influenced by the price of the processing elements (PEs) and the communication links. Thus, the design of the interconnection network topology has a crucial impact on the network cost and performance. Many topologies of interconnection networks have been presented to be used as basic modules in building MPC systems. However, the earlier topologies showed a lack of performance in case of increasing the size of the interconnection network. As a result, hierarchical interconnection networks (HINs) proposed to replace these networks. Currently, many HINs introduced to enhance the performance of MPC systems, however, we still lack a good one. In this research, a hierarchical interconnection network proposed as a basic module (BM) to build a complete parallel computer system. This topology is a completely connected network composed of six nodes and called shifted completely connected network (SCCN), also, it connected hierarchically to produce higher-levels leading to a complete system network. A two-dimensional system with multiple levels is built based on SCCN. The two-dimensional levels which composing this system are network-on-chip level, board-level, cabinet-level, and system-level. The static network performance parameters of these levels evaluated by computer simulators and the obtained results compared to multiple conventional and hierarchical interconnection networks. Moreover, in this research, we presented a three-dimensional design of SCCN based on the proposed topology. Therefore, a three-dimensional network-on-chip (3D-NoC) presented to build higher levels of 3D-SCCN. The static network performance parameters of 3D-NoC level and the higher levels assessed by computer simulators. Furthermore, the obtained results compared to other conventional and hierarchical interconnection networks. The purpose of the comparison is to prove the strength of the proposed topology which showed promising results in many aspects.

خلاصة البحث

في الوقت الحالي ايجاد جهاز كمبيوتر بديل ذو كفاءة عالية أصبح من أكثر إهتمامات الباحثين. لذلك بناء جهاز كمبيوتر قادر على تنفيذ اعداد كبيرة من الحسابات الصعبة في فترات زمنية قصيرة أصبح أمرا ملحاً. في وقتنا الحالي أنظمة الكمبيوتر المتوازية تعتبر أقوى أجهزة كمبيوتر في العالم , حيث أن وجود هذه الأجهزة هو شيء ضروري لإنجاز كثير من العمليات الحسابية في جميع المجالات وخصوصا في مجالي الهندسة والعلوم . هذه الأجهزة تم بناؤها بإستخدام شبكات تسمى الشبكات الداخلية والتي لها تصاميم محددة متمثلة في طوبولوجيا الشبكة . طبولوجيا الشبكة لها تأثير كبير على أداء هذه الشبكات وكذلك أسعار بناء هذه الشبكات مرتبط ارتباطاً وثيقاً بسعر عناصر المعالجة وأسلاك التوصيل. نستنتج من ذلك بأن تصميم الطوبولوجيا لهذه الشبكات له تأثير حقيقي على أداء وسعر تركيب هذه الشبكات . العديد من المخططات (الطوبولوجيا) للشبكات الداخلية قد تم تقديمها لتستخدم كوحدات أساسية في بناء أجهزة الكمبيوتر المتوازية ولكن الشبكات التي قدمت في الفترات الأولى أظهرت قصوراً في الأداء خصوصاً في حالة زيادة حجم الشبكات الداخلية . لذلك تم تقديم الشبكات الداخلية الهرمية لتكون بديلاً عنها في بناء أجهزة الكمبيوتر المتوازية . حاليا هناك عدد كبير من الشبكات الداخلية الهرمية قد تم تقديمها ولكن لم تثبت أي شبكة منها تفوقها على الشبكات الأخرى حتى الان . في هذا البحث شبكة داخلية هرمية جديدة قد تم تقديمها من أجل استخدامها في بناء أجهزة الكمبيوتر المتوازية . هذه الشبكة هي عبارة عن شبكة متصلة كليا ومتكونة من ستة عقد ولقد تم تسميتها شبكة الإزاحة المتصلة كليا. هذه الشبكة قد تم تقديمها لتستخدم كوحدة أساسية في بناء هذه الأجهزة الضخمة . لذلك في هذا البحث تم توصيل هذه الشبكة بصورة هرمية لإنتاج مستويات من شبكات أعلى وأكبر حجماً. وأيضاً في هذا البحث قمنا بتقديم نظام ثنائي الأبعاد , هذا النظام مبني من مجموعة مستويات قد تم انشاؤها بناءاً على شبكة الإزاحة المتصلة كلياً والتي تم تقديمها في هذا البحث . المستويات ثنائية الأبعاد التي تم تقديمها في هذا البحث تتكون من مستوى شبكة الرقاقة ,المستوى اللوحي , مستوى الخزانة , مستوى النظام الكامل. عوامل أداء الشبكة الثابتة لهذه المستويات قد تم تقييمها في هذا البحث بأستخدام محاكيات الكمبيوتر والنتائج التى تم الحصول عليها تم مقارنتها مع عدد كبير من الشبكات التقليدية والشبكات الهرمية الداخلية. أيضا في هذا البحث قمنا بتقديم التركيب ثلاثي الأبعاد من شبكة الإزاحة المتصلة كلياً. لذلك شبكة الرقاقة الثلاثية قد تم تقديمها و تم استخدامها في بناء مستويات أعلى بأعداد أكبر من العقد. أيضا عوامل أداء الشبكة الثابتة للمستويات ثلاثية الأبعاد قد تم تقييمها باستخدام محاكيات الكمبيوتر والنتائج التى تم الحصول عليها تم مقارنتها مع عدد كبير من الشبكات التقليدية والهرمية. الهدف من عملية المقارنة هو اظهار كفاءة وقوة الشبكة المقدمة من خلال هذا البحث والتى أعطت نتائج جيدة جداً في أكثر من جانب.

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DECLARATION

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LIST OF ABBREVIATIONS

SCCN	Shifted Completely Connected Network
MPC	Massively Parallel Computer
PEs	Processing Elements
HINs	Hierarchical Interconnection Networks
NoC	Network-on-Chip
VLSI	Very Large-Scale Integration
CPUs	Central Processing Units
SoC	System on Chip
2D-Mesh	Two-Dimensional Mesh
2D-Torus	Two-Dimensional Torus
TESH	Tori Connected Mesh
TTN	Tori Connected Torus Network
HTN	Hierarchical Torus Network
THIN	Triple-based hierarchical interconnection network
BSN	Block Shift Network
STTN	Symmetric Tori Connected Torus Network
3D ICs	Three-Dimensional Integrated Circuits
3D	Three-Dimensional
2D	Two-Dimensional
3D-Mesh	Three-Dimensional Mesh Network
3D-Torus	Three-Dimensional Torus Network
H3DM	Hierarchical 3D-Mesh Network
BM	Basic Module
H3DT	Hierarchical 3D-Torus Network
MH3DT	Modified Hierarchical 3D-Torus Network
3D-TESH	Hierarchical 3D Tori Connected Mesh
HTM	Hierarchical Tori Connected Mesh
NUDT	National University of Defense Technology
MIC	Many-Integrated-Core
CPEs	Computing Processing Elements
NRCPC	National Research Center of Parallel Computer Engineering and Technology
MPEs	Management Processing Elements
MC	Memory Controllers
SI	System Interface
ICs	Integrated Circuits
CGs	Core Groups
2D-SCCN	2D-Shifted Completely Connected Network
3D-SCCN	3D-Shifted Completely Connected Network
BW	Bisection Width
WC	Wiring Complexity
CEF	Cost Effective Factor
CE	Cost-Effectiveness
TCEF	Time-Cost Effectiveness Factor
3D-NoC	3D Network-on-Chip

CHAPTER ONE

INTRODUCTION

1.1 BACKGROUND OF THE STUDY

At the current time, technological advancements arose in various areas such as Artificial intelligence, Machine learning, big data, Internet of Things (IoT), autonomous robots and vehicles. Therefore, the need for super-fast systems to compute massive amounts of data in a short time increased. As a result, Massively Parallel Computer (MPC) Systems emerged to deal with the high demand of technology and to solve complicated problems in parallel by dividing the problem into parts and distribute them between thousands of CPUs and combine their results to produce an optimal and fast solution. The importance of these systems elevated because it provides power to collect, organize, and analyze big amounts of data to improve the modern life of humankind. For instance, these systems used to develop new sources of energy, improve healthcare by developing new medicines, predict and mitigate disasters, forecast weather, and many beneficial uses (Awal et al., 2014; Rahman et al., 2012) Using a single CPU core to build a computer system, make it difficult on this system to cope with the high demand of signaling technology. Moreover, sequential computers reached maximum limits to overcome many current computing problems (Sarkar, 1993; Al Faisal et al., 2016; Rahman et al., 2011). Therefore, finding an alternative solution was the priority of the research community to fulfil the new technology requirements by creating MPC systems with multiprocessor cores to replace the sequential ones. These systems considered as the high-level computer systems and used to model many difficult

problems in many areas including engineering and science (Barney, 2010). Improve the performance and reduce the cost of MPC systems is the priority of the research work. Therefore, many designs of MPC systems presented looking for an ideal one (Awal et al., 2014; Rahman et al., 2012).

The underlying interconnection network is a backbone of MPC system; these networks responsible for interconnecting the processing elements (PEs) inside the system, and it has a vital role in either improving or degrading the cost and the performance of these systems. The cost depends on the price of network devices and wires. Therefore, many research works focus on improving the performance of these networks by presenting different topologies to arrange and manage the connection between the PEs inside the system (Kim et al., 2008). The performance of these topologies evaluates based on a group of static and dynamic performance parameters to test and compare them to other topologies to find an optimal topology to be used in designing MPC systems, thus, many topologies have been proposed for this purpose. (Ali et al., 2016). Expanding the interconnection network size by increasing the number of computing nodes is the most important factor in strengthening the computing power of the system to overcome the increasing demand for computational power. The early structures of interconnection network topologies showed poor performance with the increase of the network size. Therefore, to cope with this problem, hierarchical interconnection networks (HINs) have been proposed to be an alternative solution to replace the conventional networks in building MPC systems. These networks proved their capability in increasing computing nodes number in the system to millions of nodes. Furthermore, it is an affordable way to be used in building MPC systems, and it proved proficiency in reducing power consumption. Th Therefore, a diversity of

hypercube based on hierarchical interconnection networks (HINs) proposed. However, expanding the size of these networks by adding more nodes caused large numbers of physical links and make it excessively large. To avoid this problem, numerous k-ary n-cube networks based on HINs presented such as 3D-Mesh, 3D-torus, TESH, and Cube Connected Cycles networks, however, the throughput of these networks is still very low (Al Faisal et al., 2016; Rahman et al., 2010; Rahman et al., 2009).

The rapid improvements of Very-Large-Scale-Integration (VLSI) design created a suitable environment to place a complete system in a single chip. Network-on-Chip (NoC) is an interconnection network used to connect many cores inside one chip presented as a single silicon chip to employ the communication structures of large-scale to very-large-scale integration systems (Rahman et al., 2009; Ali et al. 2016). Besides, it used to improve the communication between processors and memories inside the chip by replacing the buses and ad-hock wiring solutions of a single-core chip (Kim et al., 2005). NOC is predicted to have a promising future in improving the performance and the architecture of the future of MPC systems (Amano, 2013). The benefits of using NoC in designing large-scale systems reduce system wires complexity, control power, and provide a reliable system. The design of NoC allows the messages to flow from a source node to a destination node through numerous links that involve routing decisions at switches. Also, NoC handles synchronization issues better than the other designs. Furthermore, it provides higher operating frequencies and provides easier verification of problems due to the good design of these networks (Anagnostopoulos et al., 2009; Miura et al., 2013; Ali et el., 2016). The performance of NoC is affected by the design of the network topology which in turn affects the performance and the cost of MPC systems. Besides, the correct choice of routing protocol is important in decreasing the

network latency and congestion (Anagnostopoulos et al., 2009). Besides, the significance of hierarchical interconnection networks (HINs) is in maintaining the system performance with a high number of nodes due to its role in providing a cost-effective network. All these reasons motivated this research to propose a new topology of a hierarchical interconnection network to be as a basic module (BM) to build future generations of MPC systems. In this thesis, we will propose an architecture of a hierarchical interconnection network (HIN); this network is a completely connected network presented to enhance the performance of MPC systems. Shifted completely connected network (SCCN) is a new design of a proposed topology for Network-on-Chip (NoC) which will interconnect hierarchically to create a complete MPC system.

1.2 STATEMENT OF THE PROBLEM

The Increase of computing power and network bandwidth due to the advancements in signaling technology have motivated the researchers to find an alternative solution with special characteristics able to model complex problems in many areas (Kim et al., 2008 Development of sequential computer systems exhausted their capacity (Al Faisal et al., 2016). Therefore, to exploit the huge computing power, and yield benefits of parallelism in solving problems, supercomputers with a high number of nodes became a necessity to support technology developments of in many areas. Many problems need to be solved to build an optimum computing system. Thereby, the motivation for this research are the following problems:

1) Expand the interconnection network with thousands or millions of nodes is an infeasible with conventional interconnection networks, due to large diameter